IN THE CLAIMS

1. (Canceled)

2. (Previously presented) The method recited in claim 20, wherein the register is a control register for a data transfer operation.

3. (Previously presented) The method recited in claim 2, wherein the data transfer operation transfers data to or from a storage device.

4. (Canceled)

5. (Original) The method recited in claim 3, wherein the control register is a command register.

6. (Previously presented) The method recited in claim 20, wherein some of the bits of said register are not overwritten.

7. (Previously presented) The method recited in claim 20, wherein the data field and the bit enable field are received simultaneously.

8. (Original) The method recited in claim 7, wherein the data field is provided at an address which is contiguous with the address for the bit enable field.

9. (Previously presented) The method recited in claim 20, wherein the data transfer operation comprises a data transfer between a processor subsystem and an external storage device or peripheral.

10. (Previously presented) The method recited in claim 9, wherein the processor subsystem posts an entire command sequence for setting up the data transfer.

11. (Previously presented) The method recited in claim 9, wherein the method is carried out in a controller in a bridge connected between the processor subsystem and the external storage device or peripheral.

12. (Currently Amended) A computer comprising:

a processor subsystem;

a device which transfers data to or from said processor subsystem; and

a controller connected between said device and said processor subsystem and adapted to control the transfer of data between said device and said processor subsystem, said controller executing a method comprising,

receiving a data value of a write directed to a control register in the controller,

interpreting bits of the data value as a data field, the number of bits in the data field being equal to the number of bits in the control register in the controller and bit locations in the data field corresponding respectively to bit locations in the control register;

interpreting bits of the data value as enable bits in a bit enable field, the number of enable bits in the bit enable field being equal to the number of bits in the control register and bit locations in the bit enable field corresponding respectively to bit locations in the control register; and

overwriting only the bits at the bit locations of the control register for which the enable bit in the corresponding location in the bit enable field is set with the bit in the corresponding location in the data field, wherein the processor subsystem is to post an entire command sequence in the controller for setting up an IDE (integrated drive electronics) data transfer.

13. (Original) The computer recited in claim 12, further comprising a bridge between the processor subsystem and at least said device, the controller being included in the bridge.

14. (Previously presented) The computer recited in claim 13, wherein the device comprises an IDE (integrated drive electronics) storage device and the bridge comprises an 1/0 controller hub (ICH) which controls an IDE data transfer between the processor subsystem and the IDE storage device.

15. (Canceled) ~~The computer recited in claim 12, wherein the processor subsystem posts an entire command sequence in the controller for setting up the IDE (integrated drive electronics) data transfer.~~

16. (Previously presented) A software program stored in a tangible medium, said program, when executed, causing a computer to execute a method of writing individual bits of data to a register, said method comprising:

issuing a write of a data value to the register,

overwriting only bits at bit locations of the register for which a corresponding enable bit in the data value is set with corresponding data bits in the data value, wherein the computer is to post an entire command sequence in a controller for setting up an IDE (integrated drive electronics) data transfer.

17. (Original) The software program recited in claim 16, wherein said software program comprises a driver in the operating system software executed by a processor subsystem in the computer.

18. (Currently Amended) The software program recited in claim 17, wherein the register is a control register in [[a]] the controller adapted to control an IDE (integrated drive electronics) data transfer operation between said processor subsystem and an IDE storage device.

19. (Currently Amended) The software program recited in claim 17, wherein

the processor subsystem posts an entire command sequence for setting up the IDE (integrated drive electronics) data transfer to [[the]] a controller.

20. (Currently Amended) A method comprising

receiving data of a single write command wherein the data comprises a bit enable field and a data field comprising N bits in each field, [[and]]

updating a register with one or more bits of the data field that are associated with enabled bits of the bit enable field, and

posting an entire command sequence in a controller for setting up an IDE (integrated drive electronics) data transfer.

21. (Previously presented) The method of claim 20 wherein

the data of the single write command comprises 2*N bits,

the bit enable field comprises N bits, and

the data field comprises N bits.

22. (Previously presented) The method of claim 20 wherein the register has a location in configuration space and a location in memory space, further comprising

issuing the single write command of the data to the location in memory space for the register.

23. (Currently Amended) The method of claim 20 wherein

the ~~control~~ register has a location in I/O space and a location in memory space, and

[[the]] a processor subsystem issues a write of the data value to the location in memory space for the register.

24. (Previously presented) The method of claim 16 wherein

the data value comprises N enable bits and N data bits that correspond to N bits of the register.

25. (Previously presented) The method of claim 16 wherein

the register has a location in configuration space and a location in memory space, and

issuing a write of a data value to the register comprises issuing the write to the location in memory space for the register.